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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,625	07/22/2003	Anthony J. Benson	200300217-1	6588

22879 7590 12/21/2006
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FORT COLLINS, CO 80527-2400

EXAMINER

PARK, ILWOO

ART UNIT	PAPER NUMBER
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2182

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/624,625

Applicant(s)

BENSON ET AL.

Examiner

Ilwoo Park

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1 and 4 are amended in response to the last office action. Claims 1-16 are presented for examination.

Response to Arguments

2. Applicant's arguments filed 10/9/2006 have been fully considered but they are not persuasive. In the Remarks, Applicant argues in substance that a) Felton does not teach "a signal routing board having electronics common to circuit boards connected thereto" because figs. 7 and 8 of Felton shows a midplane 208 having a pair of power supply connectors 516, 516' which are not electronics. For this point, Felton teaches a signal routing board [midplane 208] having electronics [power supplies in fig. 8 connected to the connectors 516, 516'] common to circuit boards connected thereto and the power supplies are removable from a housing without removal of the midplane.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-9 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. [US 2003/0193776 A1] in view of Felton et al. [US 2004/0193791 A1].

As for claim 1, Bicknell et al teach an apparatus comprising:

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input/output (I/O) controller circuit boards [controller 108.1 and 108.2 in figs 1 and 7];

a storage array circuit board [e.g., intermediate electronic component 110 in fig. 6 or midplane card 112 in fig. 7] having storage device connectors to couple storage devices [disk drive 106.1-106.4] to the storage array circuit board; and

a signal routing circuit board [e.g., midplane card 112 in fig. 7 or intermediate electronic component 110 in fig. 6] having one or more connectors to couple the storage array circuit board to the signal routing circuit board, connectors to couple I/O controller circuit boards to the signal routing circuit board, and one or more multiplexers [MUX 208] to route data signals in a selective manner along one or more first data signal paths [e.g., ref. No. 206 from controller 108.1] between a first I/O controller circuit board and the storage array circuit board and along one or more second data signal paths [e.g., ref. No. 206 from controller 108.1] between a second I/O controller circuit board and the storage array circuit board, wherein the second data signal path(s) share a portion [e.g., path between MUX 208 and disk drive 106 in fig. 7] of one or more data signal paths of the first data signal path(s), wherein the signal routing board removably connects [e.g., front interface 192, rear interface 234 in figs. 5, 6] to both the I/O control circuit boards and the storage array circuit board while the storage array circuit board remains connected to a housing of the apparatus. Though Bicknell et al further disclose the signal routing circuit board [either one or midplane 112 or intermediate electronic component 110 as shown in figs. 6 and 7] providing a power [e.g., paragraphs 0029-0031] traveled from the power supply [paragraph 0016] to the storage devices and I/O

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controller circuit boards, Bicknell et al do not disclose the signal routing circuit board having one or more voltage regulators. Felton et al teach one or more voltage regulators [on a board away from a board of direct connection to the power supply in figs. 4 and 7] receiving power traveled from a power supply [fig. 2] regulates and supplies the power to at least one I/O controller circuit board and storage devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include one or more voltage regulators in order to increase reliability by supplying a stable/regulated power to I/O controller circuit boards and the storage devices of Bicknell et al.

5. As for claims 3 and 13, Bicknell et al and Felton et al teach one or more power supplies for insertion in the housing and removable coupling to the storage array circuit board or the signal routing circuit board defining one or more paths to supply power from the storage array circuit board to one or more I/O controller boards [implicit: paragraph 0017 and fig. 1 of Bicknell et al].

6. As for claims 4 and 14, Bicknell et al teach the signal routing circuit board [either one or midplane 112 or intermediate electronic component 110 as shown in figs. 6 and 7] and Felton et al teach one or more voltage regulators [on a board away from a board of direct connection to the power supply in figs. 4 and 7] to supply power at one or more levels to at least one I/O controller circuit board.

7. As for claim 5, Bicknell et al teach the signal routing circuit board defines one or more shared control signal paths to route power control and/or status signals between

the storage array circuit board and one or more I/O controller circuit boards [figs. 6-8; paragraph 0031].

8. As for claims 6 and 16, Felton et al teach the signal routing circuit board defines one or more signal paths to route signals between I/O controller circuit boards [e.g., signal line 244 in fig.2].

9. As for claim 7, Bicknell et al teach a storage system comprising:

- a housing [e.g., fig. 1];

- a storage array circuit board [e.g., intermediate electronic component 110 in fig. 6 or midplane card 112 in fig. 7] for mounting in the housing, the storage array circuit board having a plurality of storage device connectors for removably coupling a plurality of storage devices to the storage array circuit board;

- at least one input/output (I/O) controller circuit board [controller 108.1 and 108.2 in figs 1 and 7] for insertion in the housing, each I/O controller circuit board for communicating with storage devices; and

- a signal routing circuit board [e.g., midplane card 112 in fig. 7 or intermediate electronic component 110 in figs. 5 and 6] for removable connection to the storage array circuit board and with each I/O controller circuit board.

Though Bicknell et al disclose electronics [e.g., fans, power supplies, and other components in paragraph 0017] common to circuit boards, Bicknell et al do not expressly disclose the signal routing circuit board having the electronics connected thereto and removable from the housing without removal of the storage array circuit board. Felton et al teach a signal routing circuit board [e.g., midplane 208 in fig. 7]

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having electronics [e.g., power supply 112 in fig. 8] common to circuit boards connected thereto, the signal routing circuit board for removable connection to a storage array circuit board [e.g., adapter board 216 in fig. 5] and with each I/O controller circuit board [link control card 108 in fig. 2], wherein the electronics are removable from a housing without [paragraph 0024] removal of the storage array circuit board. At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of references in order to increase convenience by providing connectors to the signal routing circuit board for the electronics common to circuit boards.

10. As for claim 8, Bicknell et al teach the signal routing circuit board has one or more multiplexers [MUX 208] to route data signals in a selective manner along one or more first data signal paths [e.g., ref. No. 206 from controller 108.1] between a first I/O controller circuit board and the storage array circuit board and along one or more second data signal paths [e.g., ref. No. 206 from controller 108.1] between a second I/O controller circuit board and the storage array circuit board, and wherein the second data signal path(s) share a portion [e.g., path between MUX 208 and disk drive 106 in fig. 7] of one or more data signal paths of the first data signal path(s).

11. As for claim 9, Felton et al teach the signal routing circuit board is positioned in a generally orthogonal orientation relative to the storage array circuit board when connected to the storage array circuit board [figs. 3A and 7].

12. As for claim 15, Bicknell et al teach the signal routing circuit board defines one or more shared control signal paths to route power control and/or status signals between the storage array circuit board and at least one I/O controller circuit board [figs. 6 and 8].

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13. Claims 2, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al and Felton et al as applied to claims 1 and 7 above, and further in view of Manweiler et al. [US 6,208,522 B1].

As for claims 2 and 12, though Bicknell et al and Felton et al teach a system circuit board [e.g., host processor 106 of Felton et al in fig. 1] controlling I/O controller circuit boards through cables, Bicknell et al and Felton et al do not expressly disclose the system circuit board for removable connection to a signal routing circuit board. Manweiler et al teach a system circuit board [removable processor module 16] for removable connection to a signal routing circuit board [midplane 76 in figs. 9-12]. At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the cited references in order to increase simplicity for routing signals through the signal routing circuit board to the I/O controller circuit boards instead of plurality of cables.

As for claim 11, Manweiler et al teach a housing defines an opening [col. 4, lines 17-22] in a side for insertion of the signal routing circuit board in the housing and an opening in an end for insertion of at least one I/O controller circuit board [I/O module 36 in figs. 2 and 8].

14. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al and Felton et al as applied to claim 7 above, and further in view of Barringer et al. [US 2004/0062002 A1].

As for claim 10, Bicknell et al and Felton et al do not disclose at least one I/O controller circuit board is positioned in a generally planar orientation relative to the

signal routing circuit board when connected to the signal routing circuit board. Barringer et al teach at least one I/O controller circuit board [planar boards 14A, 14B arranged in side-by-side in figs. 1 and 6] is positioned in a generally planar orientation relative to a signal routing circuit board [midplane 28 in figs. 1 and 6] when connected to the signal routing circuit board. At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of references in order to increase flexibility in packaging of a housing.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

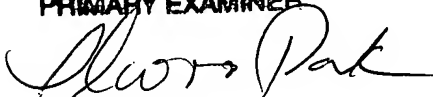
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for

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the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

A handwritten signature in cursive script, appearing to read 'Ilwoo Park', written in black ink.

Ilwoo Park

December 15, 2006